WHAT IS CLAIMED IS:

1. (Currently Amended) A manufacturing method of manufacturing a semiconductor device having a plurality of wiring layers, said method comprising the steps of:

forming a wiring by a first wiring layer as a pattern by dividing a desired pattern into a plurality of patterns, connecting the divided patterns, and exposing them, wherein a position of the connection is formed in parallel with the wiring which is formed by the first wiring layer; and

forming a wiring by a second wiring layer having an area which intersects the connecting position by a batch processing of exposure.

2. (Currently Amended) A method according to claim 1, wherein the wiring which is formed by the first wiring layer does not have an area which overlaps the connecting position and the wiring which is formed by the second wiring layer has the area which overlaps the connecting position.

3. (Currently Amended) A method according to claim 1, wherein the first wiring layer is a horizontal direction wiring layer which is parallel with the connecting position for connecting the divided patterns and the second wiring layer is a vertical direction wiring layer which perpendicularly crosses the connecting position.

4. (Currently Amended) A manufacturing method of manufacturing a solid state image pickup device having pixels each having a photoelectric converting area for converting light into signal charges and a plurality of wiring layers including a first wiring layer and a second wiring layer, said method comprising the steps of:

forming a wiring by the first wiring layer as a pattern by dividing a desired pattern into a plurality of patterns, connecting the divided patterns, and exposing them, wherein a position of the connection is arranged in parallel with the wiring which is formed by the first wiring layer; and

forming a wiring by the second wiring layer having an area which intersects the connecting position by a batch processing of exposure.

5. (Currently Amended) A method according to claim 4, wherein the wiring which is formed by the first wiring layer does not have an area which overlaps the connecting position for connecting the divided patterns and the wiring which is formed by the second wiring layer has the area which overlaps the connecting position.

6. (Currently Amended) A method according to claim 4, wherein a vertical direction wiring is formed by the first wiring layer, and a horizontal direction wiring is formed by the second wiring layer.

7. (Currently Amended) A method according to claim 6, wherein the horizontal direction wiring is a drive wiring of the pixels.

8. (Currently Amended) A method according to claim 4, wherein before the step of forming the plurality of wiring layers, a CMOS process is included at the time of the pixel creation.

9. (Currently Amended) A method according to claim 1, wherein alignment of the pattern for forming the first wiring layer and the pattern for forming the second wiring layer is made by a die-by-die system.

10. (Currently Amended) A method according to claim 4, wherein alignment of the pattern for forming the first wiring layer and the pattern for forming the second wiring layer is made by a die-by-die system.

11. (Currently Amended) A semiconductor device having a plurality of wiring layers, said device comprising:

a wiring, which is formed by a first wiring layer, formed by divisional exposure;

a connecting position at the time of the divisional exposure is formed in parallel with the wiring which is formed by said first wiring layer; and

a wiring, which is formed by a second wiring layer, having an area which intersects said connecting position.

12. (New) A manufacturing method of manufacturing a semiconductor device having a plurality of wiring layers, said method comprising steps of:

forming a wiring by a first wiring layer according to a divisional exposure, wherein the wiring formed by the first wiring layer does not intersect a connecting position at the divisional exposure; and

forming a wiring by a second wiring layer, wherein at least a part of the wiring formed by the second wiring layer has an area intersecting the connecting position.

13. (New) The method according to claim 12, wherein the wiring formed by the second wiring layer is formed according to a batch processing of exposure.

14. (New) The method according to claim 12, further comprising a step of forming a photoelectric conversion region.

15. (New) A semiconductor device comprising wirings formed from a plurality of wiring layers including at least first and second wiring layers, said device comprising:

a wiring, which is formed from the first wiring layer, formed according to a divisional exposure and not crossing over a connecting position at a divisional exposure; and

at least a part of a wiring formed from the second wiring layer crossing over the connecting position.

16. (New) The semiconductor device according to claim 15, further comprising a photoelectric conversion region.